HERMETIC PACKAGES AND FEEDTHROUGHS FOR NEURAL PROSTHESES

Quarterly Progress Report # 5

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SUMMARY

During the past quarter we continued testing the silicon-glass packages at room temperature in saline, continued testing and characterization of the wireless humidity monitoring system, prepared several glass-silicon packages with encapsulated wireless humidity monitoring systems, implanted these packages into animal hosts, studied alternate encapsulation methods for implantable prostheses, and optimized the operation of the external transmitter at 4MHz.

In the previous quarter, we mentioned that all the ongoing packages in the de-ionized water tests have failed and a lifetime of 58 years at the body temperature was estimated from these tests. Prior to this quarter, we also had 4 packages soaking at room temperature in saline as a control group to complement the accelerated tests. In this set of tests, the longest lasting package has been soaking for 1682 days, and an average soak duration for this set so far is 1370 days. All of these 4 packages are still dry and being tested. In all of our accelerated tests, we have observed the dissolution of silicon and polysilicon at the elevated temperatures. During the past quarter we have looked into etch rates versus dopant (mainly ion implanted Boron) densities at high temperatures in saline. We also looked into etch stops using different electrochemical biases by mainly a gold layer deposited on the polysilicon bonding layer. From both methods we have obtained very promising results and will incorporate these findings into the coming package fabrication run and hope to start a new set of soak tests soon.

A wireless system that consists of a hybrid coil and a polyimide relative humidity sensor had been designed and assembled together. This quarter, we have made several of these systems and have characterized their performance and behavior with respect to humidity. We have packaged a wireless system and soaked in high temperature saline and after 3 months in saline at 95°C, the humidity monitoring system (HMS) is functional and the package is still dry (confirmed with visual inspection). Few packages were made which did not have hermetic seals, and after testing in the humidity chamber we observed that they do respond linearly to changes in humidity.

One of the main accomplishments of this past quarter is the use of the wireless humidity monitoring system to monitor package integrity in-vivo. Six glass-silicon packages with HMS systems have been implanted into various locations in guinea pigs and after 1 month they all indicate that the packages are hermetic and intact. These results are very promising and we will start a few more implants soon.

We have also studied eutectic bonding and eutectic soldering as an alternative low temperature packaging method for encapsulation of implantable systems. We have achieved attachment for temperatures below 450°C, and fairly strong bonds, however the bonds have not (so far) been uniform indicating that they are also not hermetic. We will continue investigating other alternative techniques for implantable system packaging.

The external transmitter that sends power and data to the implanted systems (like microstimulator or FINESS chip) had a problem with its start up circuitry. This problem has been resolved with a simple approach. We will continue making improvements and will put the transmitter to use by testing the FINESS chips in the coming quarter.

I. INTRODUCTION

This project aims at the development of hermetic, biocompatible micropackages and feedthroughs for use in a variety of implantable neural prostheses for sensory and motor handicapped individuals. In addition, it will also develop a telemetry system for monitoring package humidity in unrestrained animals, and of telemetry electronics and packaging for stimulation of peripheral nerves. The primary objectives of the proposed research are: 1) the development and characterization of hermetic packages for miniature, silicon-based, implantable neural prostheses designed to interface with the nervous system for many decades; 2) the development of techniques for providing multiple sealed feedthroughs for the hermetic package; 3) the development of custom-designed packages and systems used in several different chronic stimulation or recording applications in the central or peripheral nervous systems in collaboration and cooperation with groups actively involved in developing such systems; and 4) establishing the functionality and biocompatibility of these custom-designed packages in *in-vivo* applications. Although the proposed research is focused on the development of the package and feedthroughs, it also aims at the development of inductively powered systems that can be used in many implantable recording and stimulation devices in general, and of multichannel microstimulators for functional neuromuscular stimulation, and multichannel recording microprobes for CNS applications in particular.

Our group here at the Center for Integrated Sensors and Circuits at the University of Michigan has been involved in the development of silicon-based multichannel recording and stimulating microprobes for use in the central and peripheral nervous systems. More specifically, during the past three contract periods dealing with the development of a single-channel inductively powered microstimulator, our research and development program has made considerable progress in a number of areas related to the above goals. A hermetic packaging technique based on electrostatic bonding of a custom-made glass capsule and a supporting silicon substrate has been developed and has been shown to be hermetic for a period of at least a few decades in salt water environments. This technique allows the transfer of multiple interconnect leads between electronic circuitry and hybrid components located in the sealed interior of the capsule and electrodes located outside of the capsule. The glass capsule can be fabricated using a variety of materials and can be made to have arbitrary dimensions as small as 1.8mm in diameter. A multiple sealed feedthrough technology has been developed that allows the transfer of electrical signals through polysilicon conductor lines located on a silicon support substrate. Many feedthroughs can be fabricated in a small area. The packaging and feedthrough techniques utilize biocompatible materials and can be integrated with a variety of micromachined silicon structures.

The general requirements of the hermetic packages and feedthroughs to be developed under this project are summarized in Table 1. Under this project we will concentrate our efforts to satisfy these requirements and to achieve the goals outlined above. There are a variety of neural prostheses used in different applications, each having different requirements for the package, the feedthroughs, and the particular system application. The overall goal of the program is to develop a miniature hermetic package that can seal a variety of electronic components such as capacitors and coils, and integrated circuits and sensors (in particular electrodes) used in neural prostheses. Although the applications are different, it is possible to identify a number of common requirements in all of these applications in addition to those requirements listed in Table 1. The packaging and feedthrough technology should be capable of:

1- protecting non-planar electronic components such as capacitors and coils, which typically have large dimensions of about a few millimeters, without damaging them;
2- protecting circuit chips that are either integrated monolithically or attached in a hybrid fashion with the substrate that supports the sensors used in the implant;
2 interfacing with structures that contain either thin-film silicon microelectrodes or conventional microelectrodes that are attached to the structure;

Table 1: General Requirements for Miniature Hermetic Packages and Feedthroughs for Neural Prostheses Applications.

Package Lifetime:

≥ 40 Years in Biological Environments @ 37°C

Packaging Temperature:

≤360°C

Package Volume:

10-100 cubic millimeters

Package Material:

Biocompatible
Transparent to Light
Transparent to RF Signals

Package Technology:

Batch Manufactureable

Package Testability:

Capable of Remote Monitoring
In-Situ Sensors (Humidity & Others)

Feedthroughs:

At Least 12 with ≤125μm Pitch
Compatible with Integrated or Hybrid Microelectrodes
Sealed Against Leakage

Testing Protocols:

In-Vitro Under Accelerated Conditions
In-Vivo in Chronic Recording/Stimulation Applications

We have identified two general categories of packages that need to be developed for implantable neural prostheses. The first deals with those systems that contain large components like capacitors, coils, and perhaps hybrid integrated circuit chips. The second deals with those systems that contain only integrated circuit chips that are either integrated in the substrate or are attached in a hybrid fashion to the system.

Figure 1 shows our general proposed approach for the package required in the first category. This figure shows top and cross-sectional views of our proposed approach here. The package is a glass capsule that is electrostatically sealed to a support silicon substrate. Inside the glass capsule are housed all of the necessary components for the system. The electronic circuitry needed for any analog or digital circuit functions is either fabricated on a separate circuit chip that is hybrid mounted on the silicon substrate and electrically connected to the silicon substrate, or integrated monolithically in the support silicon substrate itself. The attachment of the hybrid IC chip to the silicon substrate can be performed using a number of different technologies such as simple wire bonding between pads located on each substrate, or using more sophisticated techniques such as flip-chip solder reflow or tab bonding. The larger capacitor or microcoil components are mounted on either the substrate or the IC chip using appropriate epoxies or solders. This completes the assembly of the electronic components of the system and it should be possible to test the system electronically at this point before the package is completed. After testing, the system is packaged by placing the glass capsule over the entire system and bonding it to the silicon substrate using an electrostatic sealing process. The cavity inside the glass package is now hermetically sealed against the outside environment. Feedthroughs to the outside world are provided using the grid-feedthrough technique discussed in previous reports. These feedthroughs transfer the electrical signals between the electronics inside the package and various elements outside of the package. If the package has to interface with conventional microelectrodes, these microelectrodes can be attached to bonding pads located outside of the package; the bond junctions will have to be protected from the external environment using various polymeric encapsulants. If the package has to interface with on-chip electrodes, it can do so by integrating the electrode on the silicon support substrate. Interconnection is simply achieved using on-chip polysilicon conductors that make the feedthroughs themselves. If the package has to interface with remotely located recording or stimulating electrodes that are attached to the package using a silicon ribbon cable, it can do so by integrating the cable and the electrodes again with the silicon support substrate that houses the package and the electronic components within it.

Figure 2 shows our proposed approach to package development for the second category of applications. In these applications, there are no large components such as capacitors and coils. The only component that needs to be hermetically protected is the electronic circuitry. This circuitry is either monolithically fabricated in the silicon substrate that supports the electrodes (similar to the active multichannel probes being developed by the Michigan group), or is hybrid attached to the silicon substrate that supports the electrodes (like the passive probes being developed by the Michigan group). In both of these cases the package is again another glass capsule that is electrostatically sealed to the silicon substrate. Notice that in this case, the glass package need not be a high profile capsule, but rather it need only have a cavity that is deep enough to allow for the silicon chip to reside within it. Note that although the silicon IC chip is originally 500μm thick, it can be thinned down to about 100μm, or can be recessed in a cavity created in the silicon substrate itself. In either case, the recess in the glass is less than 100μm deep (as opposed to several millimeters for the glass capsule). Such a glass package can be easily fabricated in a batch process from a larger glass wafer.

The above two approaches address the needs for most implantable neural prostheses. Note that both of these techniques utilize a silicon substrate as the supporting base, and are not directly applicable to structures that use other materials such as ceramics or metals. Although this may seem a limitation at first, we believe that the use of silicon is, in fact, an advantage because it is biocompatible and many emerging systems use silicon as a support substrate.

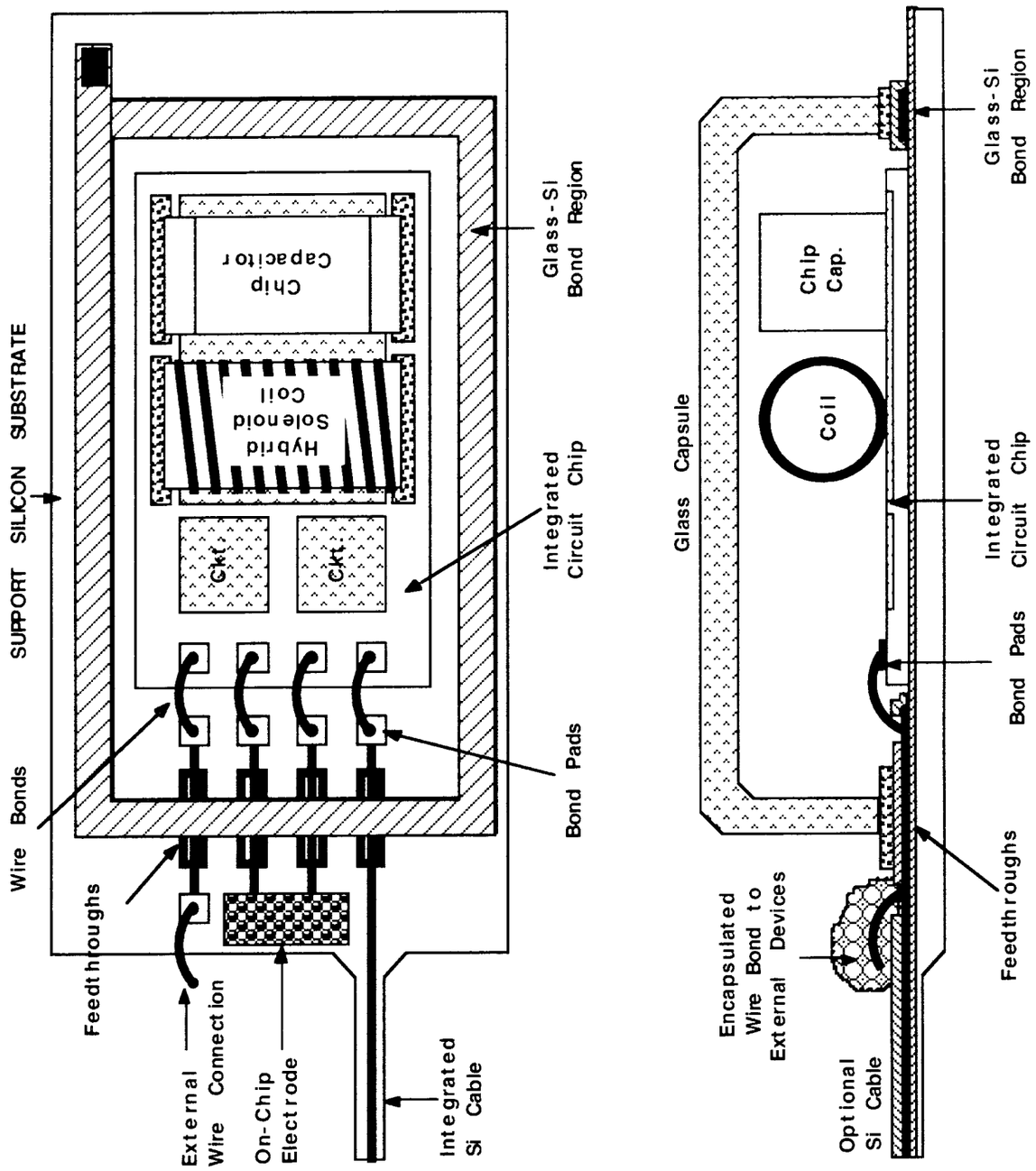


Figure 1: A generic approach for packaging implantable neural prostheses that contain a variety of components such as chip capacitors, microcoils, and integrated circuit chips. This packaging approach allows for connecting to a variety of electrodes.

We will further improve the silicon glass package and its built-in feedthroughs, and will study and explore alternative technologies for hermetic packaging of implantable systems. In particular, we have proposed using a silicon capsule that can be electrostatically bonded to a silicon substrate thus allowing the capsule to be machined down to dimensions below a 100μm. We will also develop an implantable telemetry system for monitoring package humidity in unrestrained animals for a period of at least one year. Two separate systems have been proposed, one based on a simple oscillator, and the other based on a switched-capacitor readout interface circuit and an on-chip low-power AD converter, both using a polyimide-based humidity sensor. This second system will telemeter the humidity information to an outside receiver using a 300MHz on-chip transmitter.

Finally, we have forged potential collaborations with two groups working in the development of recording/stimulating systems for neural prostheses. The first group is that led by Professor Ken Wise at the University of Michigan, which has been involved in the development of miniature, silicon-based multichannel recording and stimulation system for the CNS for many years. Through this collaboration we intend to develop hermetic packages and feedthroughs for a 3-D recording/stimulation system that is under development at Michigan. We will also develop the telemetry front end necessary to deliver power and data to this system. The second group is at Case Western Reserve University, led by Prof. D. Durand, and has been involved in recording and stimulation from peripheral nerves using cuff electrodes. Through this collaboration we intend to develop a fully-integrated, low-profile, multichannel, hermetic, wireless peripheral nerve stimulator that can be used with their nerve cuff electrode. This system can be directly used with other nerve cuffs that a number of other groups around the country have developed. Both of these collaborations should provide us with significant data on the reliability and biocompatibility of the package.

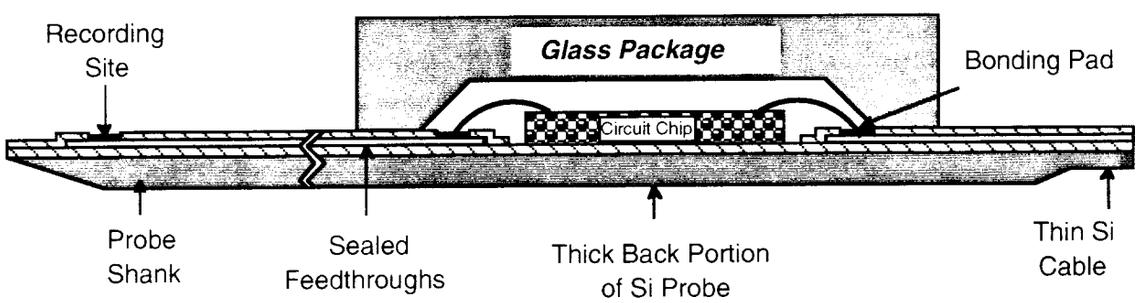


Figure 2: Proposed packaging approach for implantable neural prostheses that contain electronic circuitry, either monolithically fabricated in the probe substrate or hybrid attached to the silicon substrate containing microelectrodes.

II. ACTIVITIES DURING THE PAST QUARTER

2.1 Hermetic Packaging

Over the past few years we have developed a biocompatible hermetic package with high density multiple feedthroughs. This technology utilizes electrostatic bonding of a custom-made glass capsule to a silicon substrate to form a hermetically sealed cavity, as shown in Figure 3. Feedthrough lines are obtained by forming closely spaced polysilicon lines and planarizing them with LTO and PSG. The PSG is reflowed in steam at 1100°C for 2 hours to form a planarized surface. A passivation layer of oxide/nitride/oxide is then deposited on top to prevent direct exposure of PSG to moisture. A layer of fine-grain polysilicon (surface roughness 50Å rms) is deposited and doped to act as the bonding surface. Finally, a glass capsule is bonded to this top polysilicon layer by applying a voltage of 2000V between the two for 12 minutes at 320 to 350°C, a temperature compatible with most hybrid components. The glass capsule can be either custom molded from Corning code #7740 glass, or can be batch fabricated using ultrasonic micromachining of #7740 glass wafers.

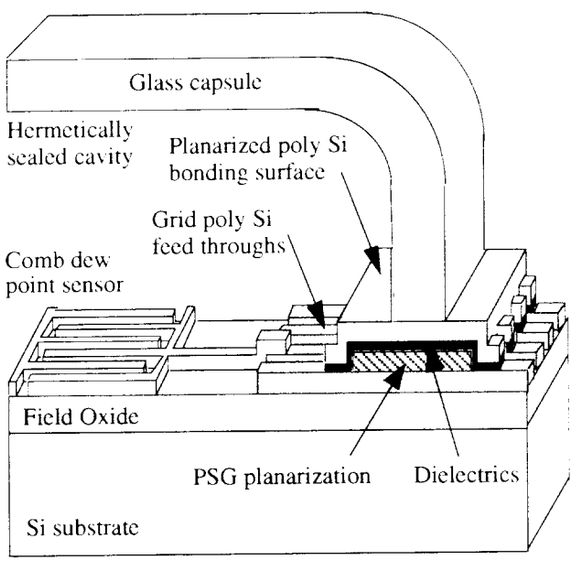


Figure 3: The structure of the hermetic package with grid feedthroughs.

During the past few years we have electrostatically bonded and soak tested over one hundred and sixty of these packages. The bonding yield is about 82% (yield is defined as the percentage of packages which last more than 24 hours in the solution they are soaked in). At the beginning of this quarter 4 devices were still being tested in saline at room temperature. These devices have been under test for more than 4.5 years and show no sign of leakage. We should mention that these devices have been made with silicon substrates that are thinned (~150μm) and bonded to the custom molded glass capsules. During this term, we have characterized the etch rates of Boron doped Silicon and also Silicon protected with an electrochemical bias namely with a Au layer in saline at elevated temperatures. We were able to reduce the dissolution rates by 2 orders of magnitude and will hence start a new set of high temperature soak tests. We have also continued fabrication of silicon substrates and also started several in-vivo tests using a wireless humidity sensor-hybrid coil system.

2.1.1 Ongoing Room Temperature Soak Tests in Saline

The packages soaked in phosphate buffered saline at room temperature have been under test for more than 4.5 years now. These soak tests were started to complement the accelerated soak tests at the higher temperatures. Furthermore, upon close inspection of the top polysilicon layer, it is found out this top layer is there and is not etched after 4.5 years of testing. Our conclusion is that at room temperature we are below the activation energy required to cause dissolution of polysilicon and hence we have not yet observed any dissolution related failures. This observation is in accordance with the acceleration model used in interpreting the high temperature tests. Indeed, it seems to confirm that the activation energy for the dissolution of the substrate or the top polysilicon is high. Accordingly, due to the exponential decrease of the acceleration factor with temperature, the dissolution of silicon or polysilicon may not be significant at the body temperature.

Out of the original 6 packages, one failed prematurely the first day and one failed because of mishandling. The 4 other devices are still under test and present no sign of leakage into the capsule after being soaked for 1682 days. Table 2 summarizes the data obtained from these soak tests.

Table 2: Data for room temperature soak tests in saline.

Number of packages in this study	6
Soaking solution	Saline
Failed within 24 hours (not included in MTTF)	1
Packages lost due to mishandling	1
Longest lasting packages in this study	1682 days
Packages still under tests with no measurable room temperature condensation inside	4
Average lifetime to date (MTTF) so far including losses due to mishandling	1370 days
Average lifetime to date (MTTF) so far excluding losses due to mishandling	1673 days

2.2 Polysilicon Corrosion Prevention in High Temperature Saline

As mentioned in previous quarterly reports, the dissolution of silicon/polysilicon has been a major obstacle in conducting accelerated soak tests. Our goal is to stop this dissolution and look for other failure modes if they exist and obtain lifetime data on glass-silicon packages for encapsulation of implantable systems. In the previous quarterly report we indicated that Boron doping via ion implantation can be used to stop the dissolution of polysilicon. We have chosen ion implantation because Boron doping which is routinely used to create etch stop layers for the Silicon probes and alike is done at a high temperature for long durations which in turn increases the surface roughness to an unacceptable level for hermetic bonding. Hence to learn more about the etch rates of Boron implanted Silicon in high temperature saline, we prepared several wafers, ion implanted them and soaked them at high temperatures to obtain etch rates and also characterized the surface roughness arising from Boron implantation.

The sample set consists of 8 silicon wafers that are oxidized with a 920nm thick polysilicon layer deposited on top. The wafers are doped with different doses and energies. In general, the dose determines the amount of dopants in Silicon and the energy determines the depth the dopants reside. This sample set is summarized in Table 3.

Table 3: The parameter table for the ion implanted wafers.

Number of Wafers	Dose (cm^{-2})	Energy (KeV)
3	1e16	90
2	1e15	90
3	1e14	140

Using a simulation program we determined that an anneal of 6 minutes at 1100°C is sufficient to uniformly distribute the dopants in the 920nm thick polysilicon layer. So, after receiving the ion implanted 4" wafers, we diced them into small squares of 1cm on each side and then annealed them using a rapid thermal annealer. The samples are next soaked in jars containing phosphate buffered saline (PBS) at 93°C and 91°C. Furthermore, we have attempted to protect polysilicon etching using an electrochemical etch stop [1] and hence sputtered a layer of Cr/Au on one corner of several samples. The results of these experiments are shown in Table 4.

Table 4: Etch rates of doped/implanted polysilicon w/o an electrochemical bias in PBS.

Temperature	Boron implanted no bias	Boron implanted with Au electrode	Phosphorus doped with Au electrode	Phosphorus doped no bias
93°C	90Å/Day	86Å/Day	82Å/Day	> 10,000Å/Day
91°C		72Å/Day	71Å/Day	> 10,000Å/Day

The above results indicate that at each temperature there is a small but finite etch rate for polysilicon (Boron implanted, Boron implanted with Au electrode, Phosphorus doped with Au electrode) in PBS. From our control samples (Phosphorus doped with no bias) we find that the etch rate of undoped polysilicon or polysilicon with residual Phosphorus doping is more than 10,000Å per day. At these elevated temperatures it appears that both Boron doping and also Au coating reduces the etch rates by close to 2 orders of magnitude. With these etch rates we are confident that we can conduct longer studies and determine other failure modes for the package without being effected by the finite etch rate of the polysilicon layer.

The abovementioned polysilicon layer is the top bonding polysilicon layer hence the surface roughness is of critical importance in achieving a hermetic seal. To investigate the surface roughness of the Boron implanted polysilicon we have examined the samples under a Scanning Electron Microscope. After inspecting the surfaces of undoped polysilicon and Boron implanted and annealed polysilicon under very high magnification, we did not observe any doping generated roughness since both samples looked very similar. To obtain a more quantitative data, we have taken another set of 2 samples and have inspected their surfaces using an Atomic Force Microscope. Figures 4 and 5 show the surface profiles from these samples. As with the SEM inspection, the samples look very similar. The rms surface roughness of the undoped sample is 80Å and the Boron doped and implanted one is about 100Å. These values correspond to the area that is scanned (5 micron x 5 micron) and with these close rms values for the samples, it is clear that the additional surface roughness generated by the implantation and anneal combination is not significant and hence this new procedure can be readily employed into the package substrate fabrication. Currently we have 2 wafers that are being processed and we will dope these wafers with Boron and also add an electrochemical bias with a Au layer at one edge so that we will have maximum possible protection and will soon start a new batch of soak tests utilizing the recently developed wireless humidity sensing system which will be detailed in the following section.

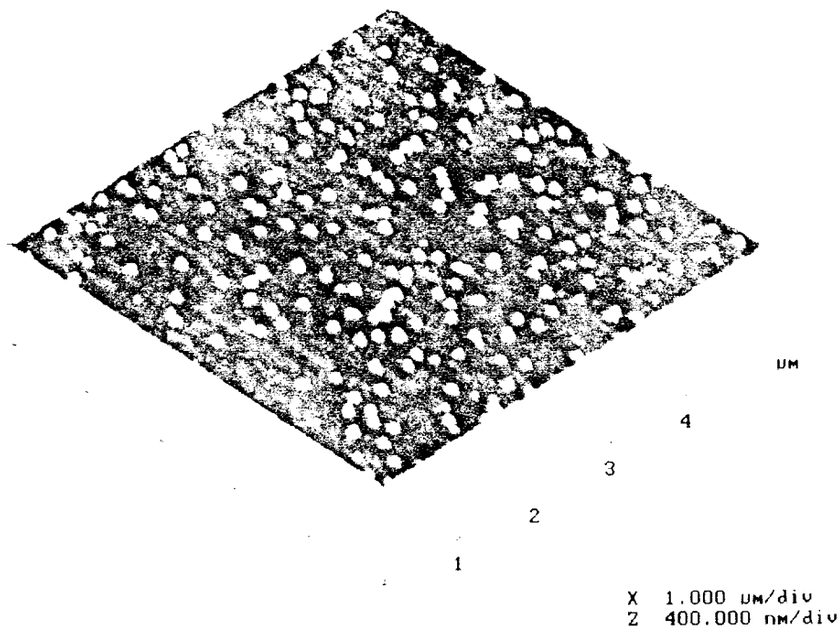


Figure 4: The surface profile of the polysilicon layer as deposited obtained using AFM.

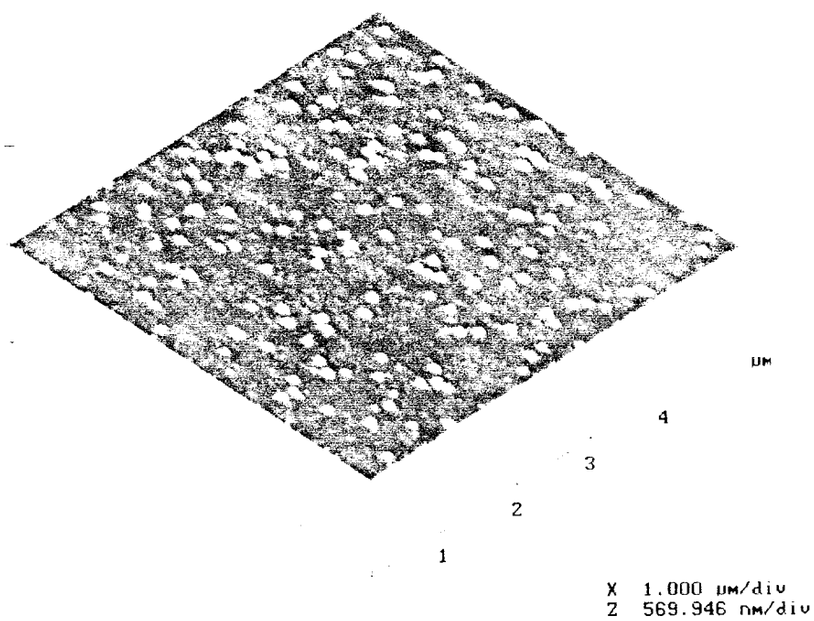


Figure 5: The surface profile of the Boron doped and annealed polysilicon layer as deposited obtained using AFM.

2.3 Wireless Monitoring of Humidity Inside Glass-Silicon Packages

The use of a wireless humidity monitoring system (HMS) for package testing and monitoring has several benefits. It greatly facilitates the in-vitro testing of the packages, decreases the detection threshold of moisture, reduces mishandling and temperature cycles, allows one to automate the in-vitro testing procedur, and allows continuous monitoring of humidity in packages that are implanted in animal hosts, thus providing us with important in-vivo hermeticity data.

In the previous quarterly report, we explained the approach that we have chosen. The approach can be summarized as the following: a capacitive polyimide humidity sensor (HS) is wire bonded to an inductor made by copper wires wound around a ferrite core. This coil with the HS forms a LC tank circuit. The capacitive humidity sensor in this tank circuit responds to changes in humidity by changing its capacitance and thus the resonance frequency of the tank circuit shifts. When another coil (external antenna) is placed nearby this tank circuit; the maximum loading in the impedance measurements of the antenna is observed at the resonance frequency of the tank circuit allowing one to remotely monitor changes in humidity levels. We thus call the HS and the inductor combination the Humidity Monitoring System (HMS).

2.3.1 System configuration

The wireless monitoring system consists of an external loop antenna (of inductance L_a), inductively coupled to the humidity monitoring system (HMS). The HMS is a hybrid copper wire coil (with inductance L and series resistance R) wire bonded to a humidity sensor (with capacitance C varying with humidity). The hybrid coil inside the package is modeled as a solenoid (a valid approximation, however, the actual coil has a rectangular shape) and for simplicity, we assume that the antenna coil and the HMS coil are coaxial.

The schematic of the system is shown in Figure 6 and the equation parameters for this system are given in Table 5.

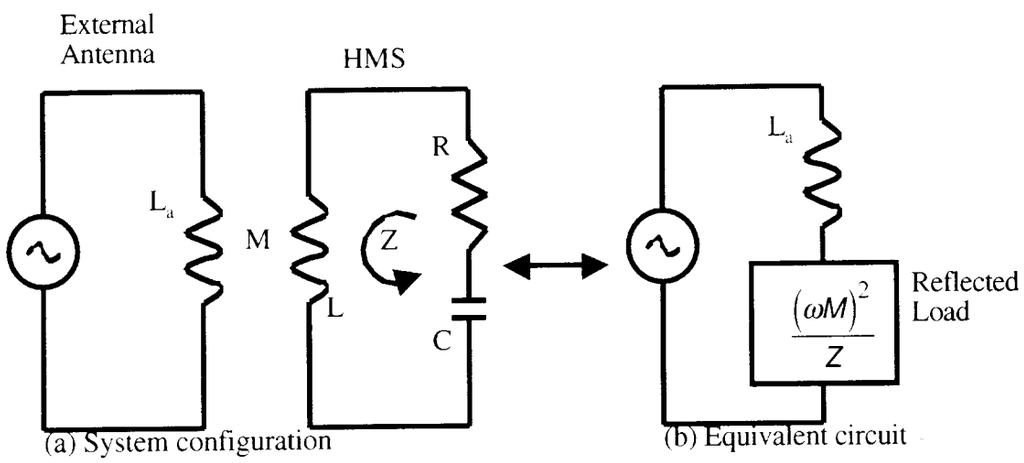


Figure 6: The schematic of the humidity monitoring system.

Table 5: Equation parameters for the HMS.

Antenna:		Humidity Monitoring System:	
L_a	self-inductance (H)	L	coil self-inductance (H)
a	radius (m)	d	coil diameter (m)
N_a	number of turns	l	coil length (m)
μ_0	permeability (4πe-7 Ohms/m)	S	cross sectional area (m^2)
		$\mu=\mu_0\mu_r$	magnetic permeability
Coupling:		μ_r	relative permeability of the core
M	mutual inductance	C	capacitance of the humidity sensor
z	axis distance	R	series resistance

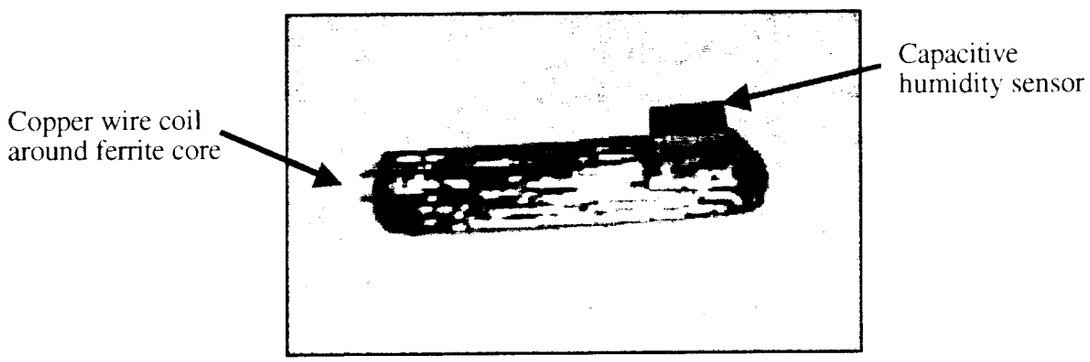


Figure 7: An assembled HMS.

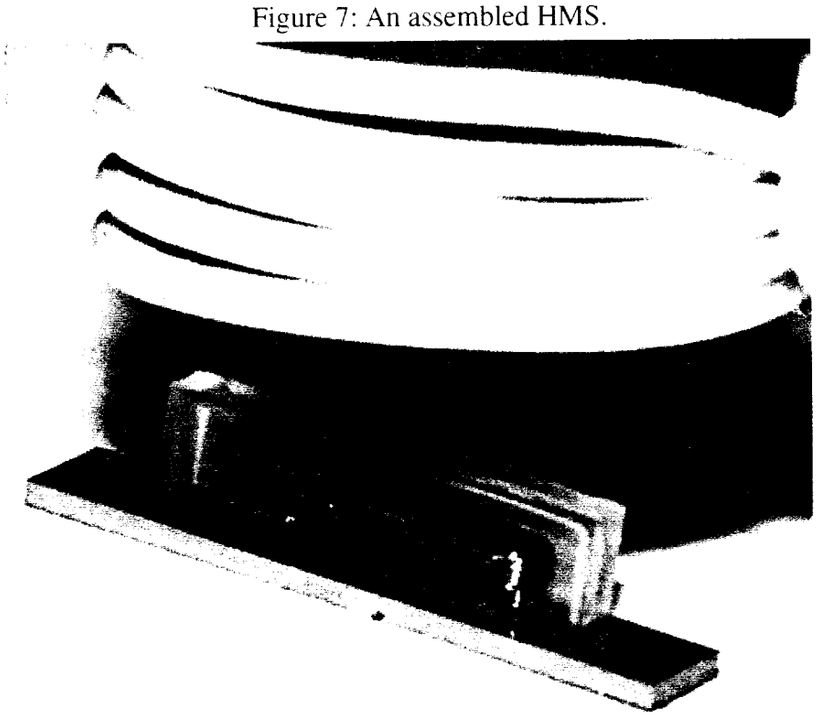


Figure 8: External antenna and half-diced glass on a silicon substrate with enclosed HMS.

Figure 7 shows a HMS to be used to test the hermeticity of glass-Si anodic bonding. Figure 8 shows the antenna testing setup with a half diced glass capsule revealing the HMS inside.

2.3.2 Ferrite Core Loop Antenna

Ferrite core loop antennas are studied in order to improve the sensitivity and the range of the wireless system. From the last quarterly report (April '99) it is shown that the impedance of the antenna at resonance is

$$Z_{resonance} = \frac{\omega^2 \cdot M^2}{R} + j \cdot L_a \cdot \omega$$

where the mutual inductance is

$$M(z) = \frac{\mu \cdot a^2 \cdot N \cdot S}{2(a^2 + z^2)^{3/2}} [Henry]$$

and the antenna inductance is

$$L_a = \frac{\pi \cdot \mu \cdot N_a^2 \cdot a}{2}$$

The reflected load impedance of the HMS is the real part of the expression for $Z_{resonance}$. Therefore, to have the maximum phase dip (or highest sensitivity) the following ratio should be maximized.

$$\frac{\mathrm{Re}(Z_{resonance})}{\mathrm{Im}(Z_{resonance})}$$

Using a ferrite material in the antenna core allows the permeability μ to be increased by a factor μ_r (μ_r is determined by the ferrite material characteristics). Therefore, for a ferrite loaded loop antenna, the real part of $Z_{resonance}$ is increased by a factor of μ_r^2 and the imaginary part by μ_r thus the sensitivity of the antenna is increased. Figure 9 shows the response of an antenna with a ferrite core and with an air core.

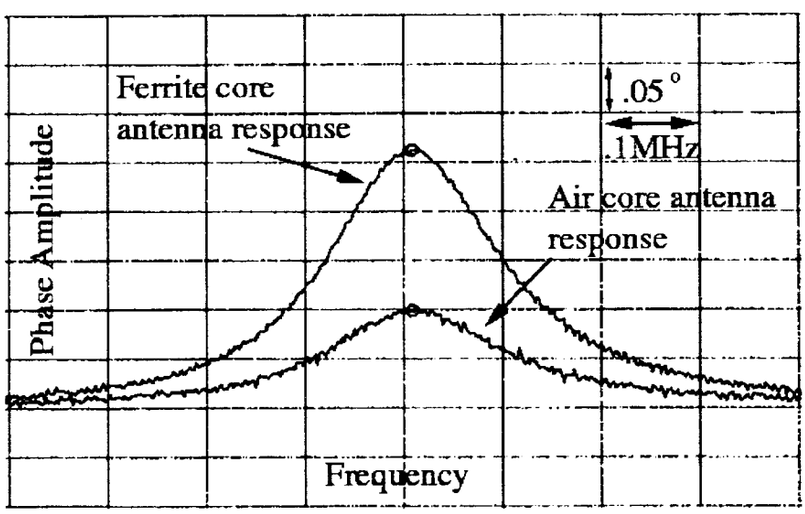


Figure 9: Phase amplitude of ferrite loaded and non-ferrite loaded antenna.

The measurements are conducted using the same antenna with a 0.5" loop diameter and at a fixed separation distance of 1cm from the Silicon-glass package with an enclosed HMS.

One drawback to using ferrite core loop antennas to test the HMS is that at close distances the phase response is shifted in frequency as shown in Figure 10.

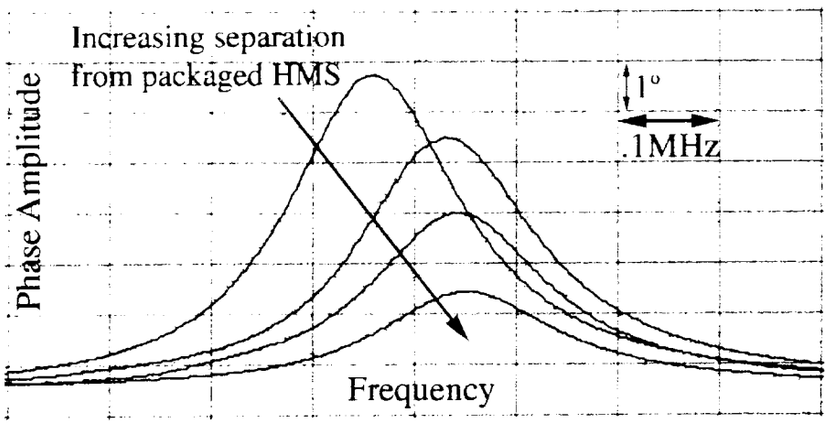


Figure 10: Phase amplitude frequency shift with ferrite loaded antenna.

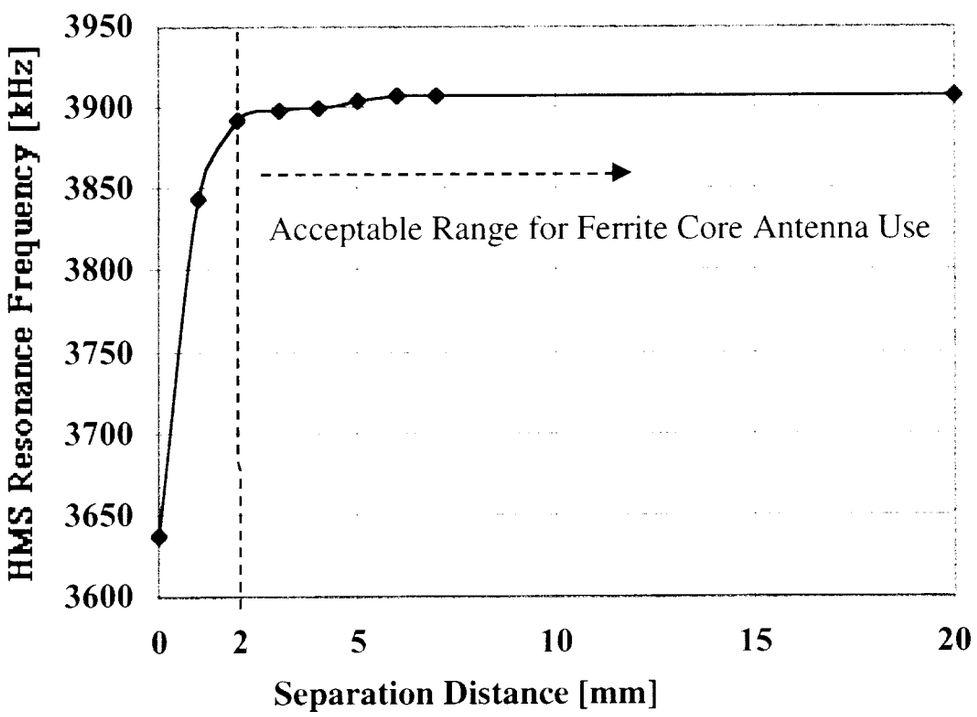


Figure 11: Frequency shift data for ferrite loaded loop antenna.

This frequency shift is attributed to the increased magnetic field of the ferrite core antenna on the HMS ferrite core inductor coil. The permeability of a ferrite material is nonlinearly proportional to the magnetic field impressed upon it. Therefore as the antenna moves closer to the HMS the magnetic field through the HMS ferrite core copper wire coil increases. This increases the permeability of the HMS ferrite and thereby increases the coil inductance. Since the resonant frequency of the HMS is

$$f_{resonance} = \frac{1}{2\pi\sqrt{LC}}$$

a decrease in resonant frequency is observed when the ferrite antenna is brought closer to the HMS. While these ferrite antennas should not be used for testing at separation distances of less than 2mm (as shown Figure 11), they may be used at distances in the range of 2mm to 2cm (beyond 2cm the signal becomes too weak to detect). This is an improvement because air core antennas are only useful up to 1cm from the HMS. Increased antenna sensitivity of ferrite core antennas allows extended testing distances, which may be useful for animal implant testing.

2.3.3 HMS Response Inside a Non-Hermetically Bonded Glass-Si Package

A glass silicon package is anodically bonded to a silicon substrate with an HMS enclosed. The bonding region is inspected under a microscope and it is observed that a portion of the glass is not hermetically sealed to the silicon. Figure 12 shows the bonded and unbonded regions of the device. This device is placed in a humidity chamber to test the response of the HMS in a non-hermetic glass-Si package. The HMS data is provided in Figure 13. It is confirmed that the HMS can accurately detect non-hermeticity of the glass-silicon packages.

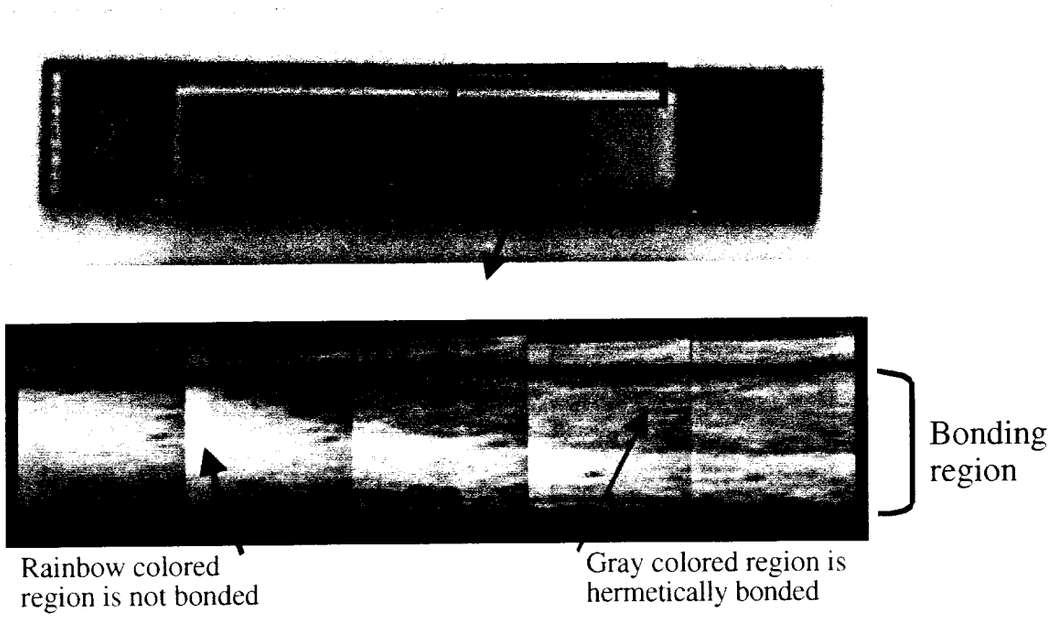


Figure 12: Bonding region of tested glass-Si package.

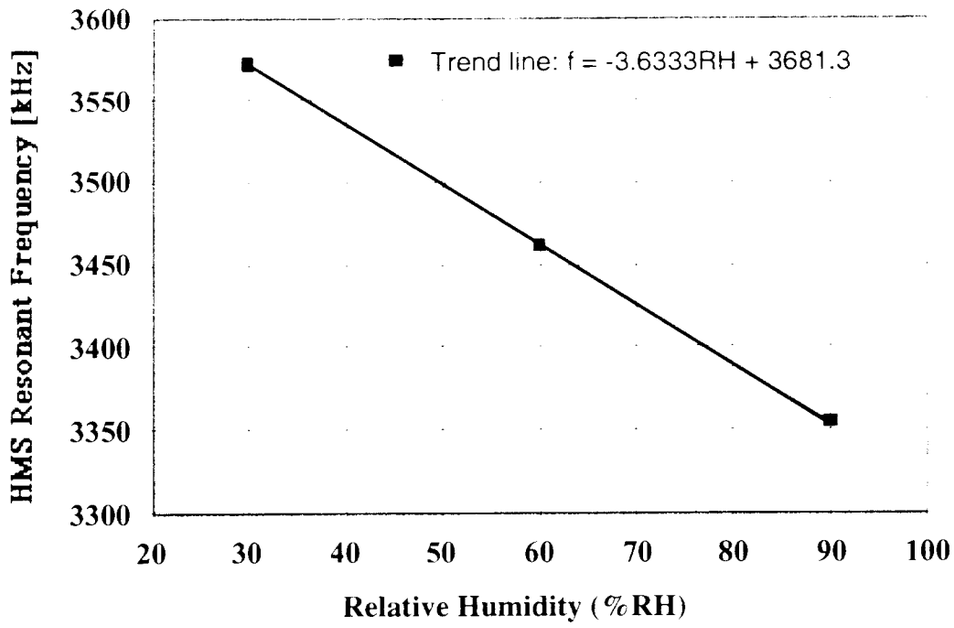


Figure 13: Humidity data of non-hermetically bonded glass-Si package.

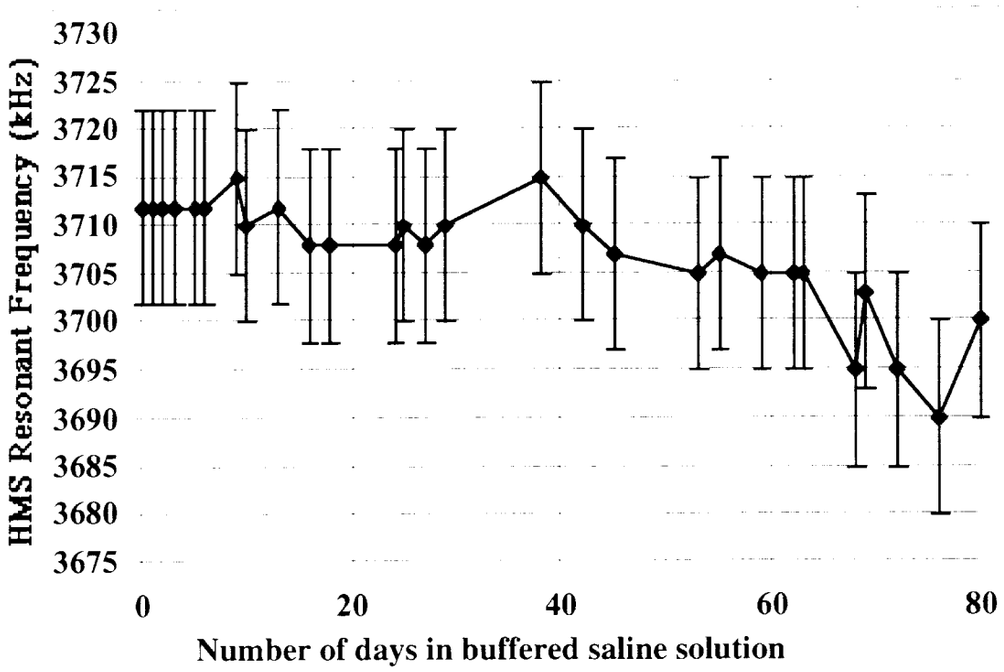


Figure 14: Telemetry data from a package soaked in high temperature saline soak test (95°C).

2.3.4 High Temperature Soak Test in Saline

An anodically-sealed Humidity Monitoring System (HMS) has been soaking since April 1999 in phosphate buffered saline solution at high temperature of around 95°C. The package is inspected routinely under a microscope to detect any leakage path(s) on the bonding surface, and the resonant frequency of the HMS is measured to correlate this response with the humidity inside the sealed package. This data may provide useful information as to the failure and degradation processes of the package hermeticity. As of mid July, neither a complete leakage path and nor a corresponding frequency shift has been observed. On the previous page, Figure 14 shows the measured frequency versus the number of days soaking at 95°C, with a y-axis margin error of 10 kHz (~ 2%RH) on the detection of the HMS resonant frequency.

The frequency variations are attributed to day to day temperature fluctuations during testing. These variations are within experimental error and hence the HMS data and visual inspection analysis strongly suggest the anodically-sealed package is hermetic.

2.3.5 Calibration Procedure of Humidity Monitoring System (HMS)

Humidity Monitoring Systems are always calibrated before being anodically bonded. The high temperature and the high electric field during bonding may affect the calibration (offset and slope) of the HMS. Furthermore the inductor and the polyimide humidity sensor can also be effected by this extremely high field, if not properly placed, as well as the temperature. Accordingly, a sample HMS has been utilized to observe the effects of anodic bonding on the HMS both at the component level and the system level. In order to explore the effects of bonding, if any exist, the HMS needs to be carefully characterized prior to anodic bonding. We have reported the behavior of the humidity sensor before and after a heat cycle of 400°C for 1 hour, however this is the first time that this polyimide sensor and the enclosed coil are being exposed to the high electric fields generated during anodic bonding. After the HMS is assembled, the following steps are performed in this experiment:

(i) Pre-bond annealing for 30-60 minutes at 350°C.
(ii) Calibration in the humidity chamber at 37°C (for in-vivo implant devices) or at 25°C (for room temperature tests) at 30, 50 and 70%RH as seen in Figure 15 and the measured resonant frequencies are carefully recorded.
(iii) The Glass-Si package is bonded with the HMS enclosed at 350°C.
(iv) The frequency response is measured at room temperature. The measured frequency should be higher than any frequencies recorded during pre-bonding calibration, due to the fact that during bonding more humidity is driven out of the RH sensor which results in a decrease in capacitance and an increase in the resonant frequency of the HMS.

A sample HMS is used to study the accuracy of the calibration. This prototype humidity monitoring system was annealed at 260°C on a hot plate for 1 hour (it would be better from now on to use a slightly higher annealing temperature as suggested in the calibration procedure above because a difference in pre-bond curing temperature and the anodic bonding temperature causes a larger offset in resonance frequency measured before and after bonding). The resonant frequency is measured in the humidity chamber at 37°C at different humidity points, which gives the pre-bonding calibration curve in Figure 16. The humidity system is then placed in a glass capsule and anodically bonded to a silicon substrate. After bonding, the glass capsule was broken to expose the HMS to the humidity chamber environment and perform post-bonding measurements. We have obtained resonance frequencies expected of a further dried (of moisture) polyimide sensor with a lower capacitance. Another reason that the capacitance has decreased is the low relative humidity level at the sealing temperature of 350°C. The HMS system performed as expected and there was no indication of a damage caused by heat or high fields. Figure 16 compares the pre-

and post-bonding calibration curves. As expected further curing during anodic bonding results in a smaller capacitance which in turn results in a larger resonance frequency as mentioned in previous reports on characterization of the RH sensor.

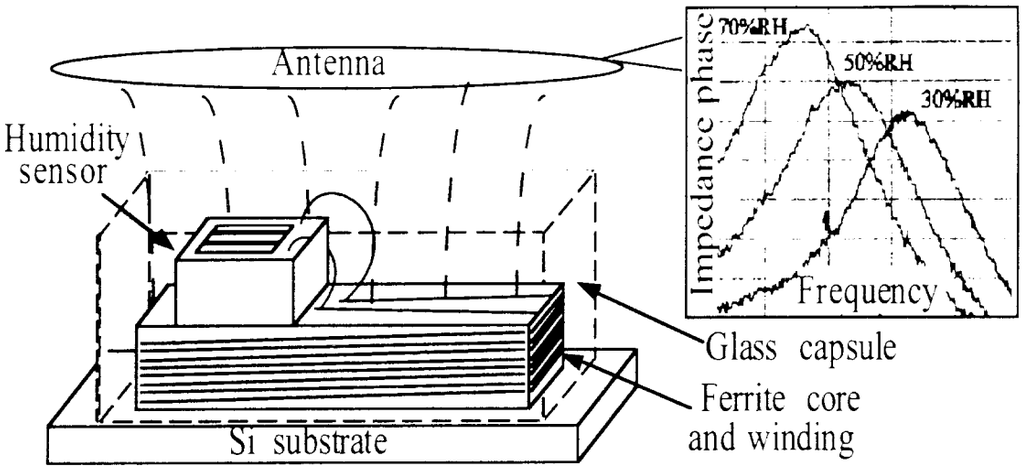


Figure 15: Humidity sensing system with the external antenna on top.

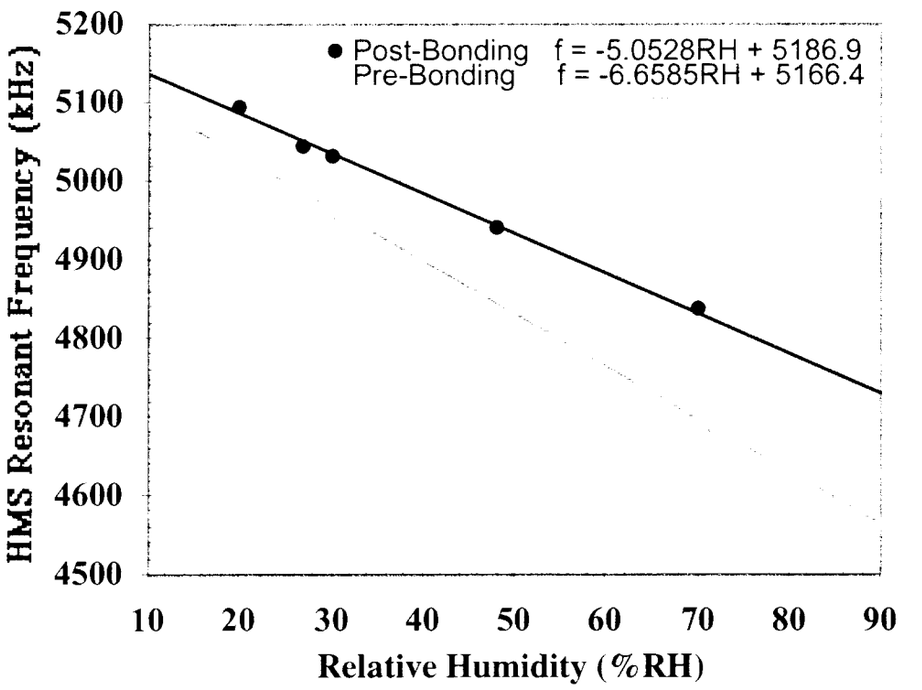


Figure 16: Pre/Post-bonding calibration data.

2.4 Leak Testing

Prior to the start of a new high temperature soak test, we decided to inspect the quality of the bonding surface from a recent processing run by doing both a complete surface topography analysis, and by doing a leak check after a few packages are made. A new optical surface profiler has just been bought and is recently being set up in our cleanroom for surface analysis and will be utilized in the future. In order to ensure that the packages are holding a hermetic seal, it is necessary to conduct fine and gross leak testing. These tests are designed to detect gas leaks from packages. The gross leak test is conducted by immersing the package in a chamber filled with water. The package is examined under a microscope to look for any bubbles. This test is necessary to guarantee that the fine leak test will have conclusive results. A package that fails a gross leak test responds to a fine leak test very rapidly giving incorrect results. The fine leak test is conducted by placing the package in a pressurized (4 atmospheres) chamber filled with helium and a radioactive tracer gas. The package is then placed near detection equipment that measures the release of the gas from the package. Using these techniques, leak rates down to 10^{-9} atm-cm^3/s are detectable. According to MIL-STD-883, the high reliability electronic parts standard, a package of the volume being tested may be considered hermetic if the leak rate is less than $5x10^{-8}$ atm-cm^3/s. This test should determine if our packages meet high reliability standards for hermetic seals.

Since this test requires experienced personnel operating calibrated equipment, it was decided that these tests should be conducted at an external facility. As such, five packages were prepared and shipped to NASA's Jet Propulsion Laboratory for testing. The Electronic Parts Engineering Section of the Jet Propulsion Laboratory, in the interests of learning more about hermeticity of the novel micromachined packages, has agreed to perform this test at no charge to the University of Michigan. While, as of the time of this report, the test results have not been received, they are expected within the next few weeks and will be reported in the coming report.

2.5 In-Vivo Testing

With the development of the wireless humidity monitoring system, it is now possible to remotely monitor package integrity while the device is implanted in an animal host. Consequently, six devices were prepared and screened to insure hermetic seals. Each device passed a one-day room temperature soak in DI water to validate the seal prior to implant. The devices were then sent to the University of Michigan Medical School for implantation into guinea pig hosts. Two guinea pigs have been implanted with packages to monitor hermeticity in the in-vivo environment. Sites on the guinea pigs were selected to give the widest possible range of environmental conditions. On each host, one package was implanted into the leg, another into the abdomen, and a final one into the head for a total of three packages per host. Devices in the head were implanted beneath the skull but above the dura as shown in Figure 17. Devices in the leg were implanted under the skin on top of the leg muscles as illustrated in Figure 18. Devices in the abdomen were implanted in the abdominal cavity as depicted in Figure 19.

Tests were conducted immediately prior to and following implant, with no discernible change in system output. After this, devices were measured twice weekly to detect shifts in resonant frequency resulting from changes of humidity in the package if any. The implants were performed on the first animal on June 23 and for the second animal on June 30. This gives a running total of three weeks of testing on the first animal and two weeks of testing on the second animal. As of July 19 there has been no discernible shift in the output of any humidity sensing systems inside the packages. Given that a 50 kHz shift is considered significant, the output of the sensors, which varies by only a few kilohertz, indicates fairly steady humidity inside the packages. Figures 20 and 21 show the measured frequencies of the sensors over the duration of the test.

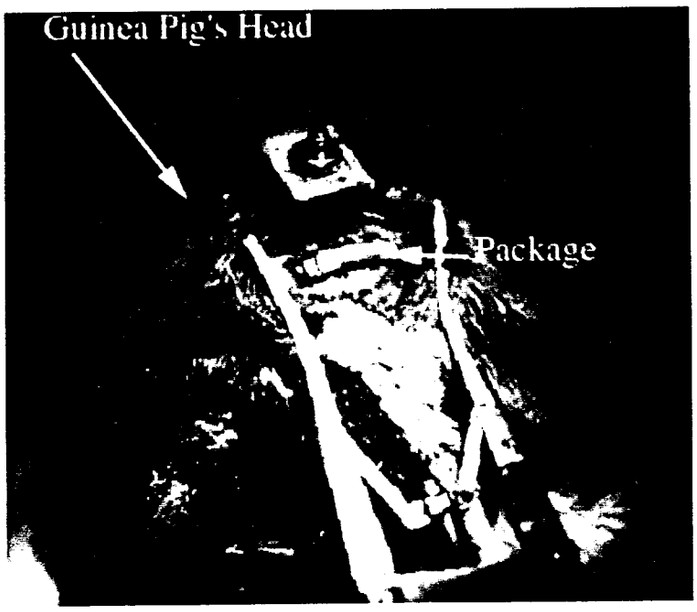


Figure 17: Head of a guinea pig with the implanted package.

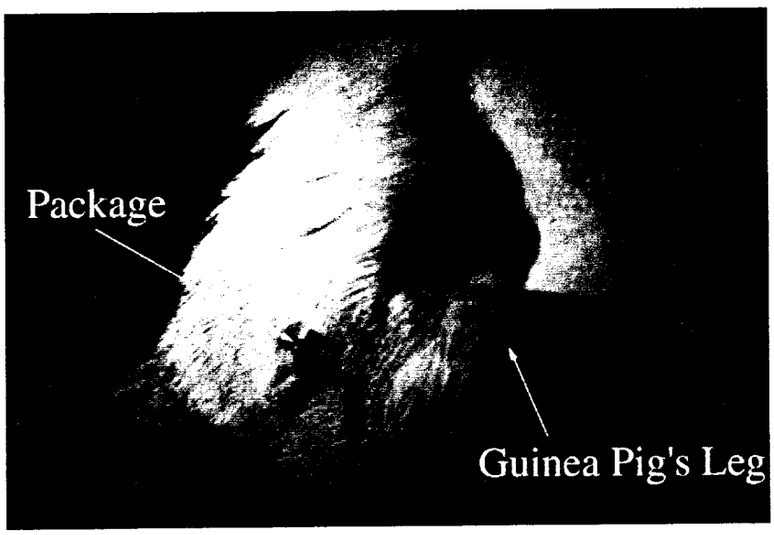


Figure 18: The photograph of the guinea pig's leg with the implanted package.

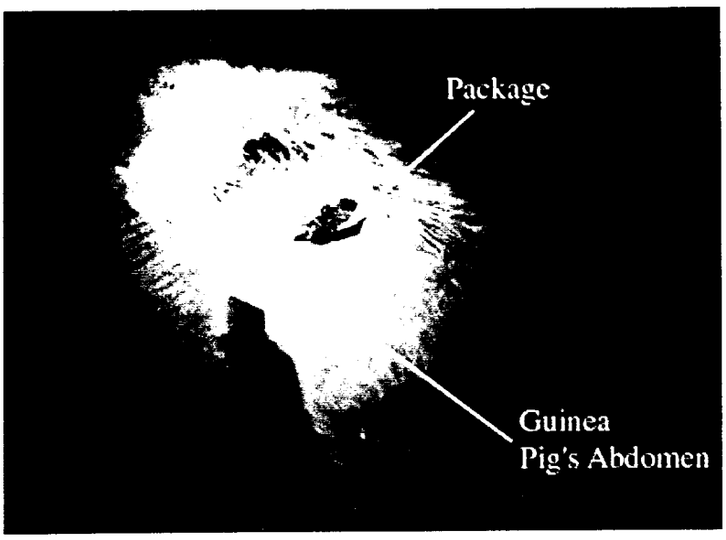


Figure 19: The photograph of the guinea pig's abdomen with the implanted package.

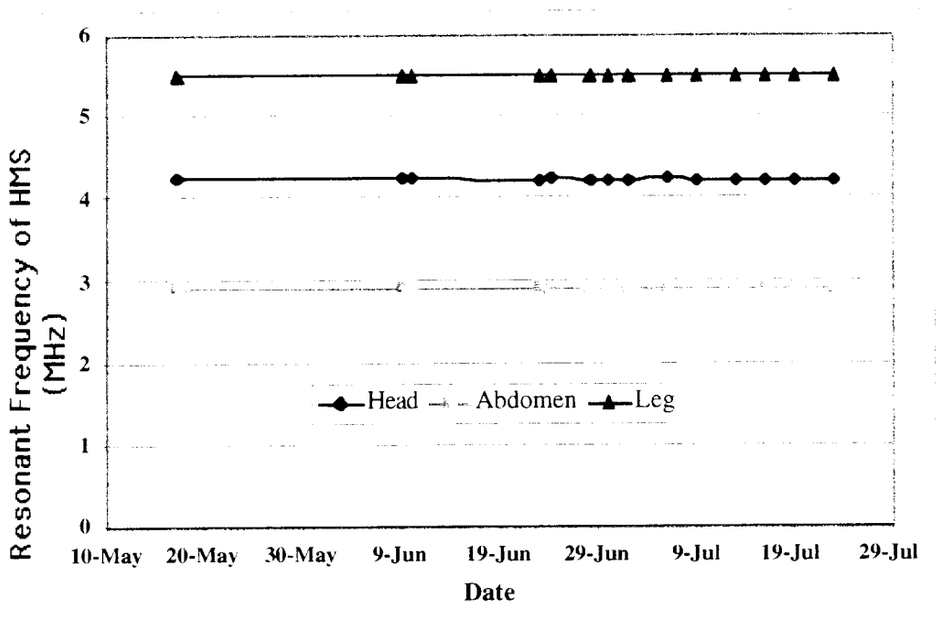


Figure 20: Humidity measurements over time for Guinea Pig A.

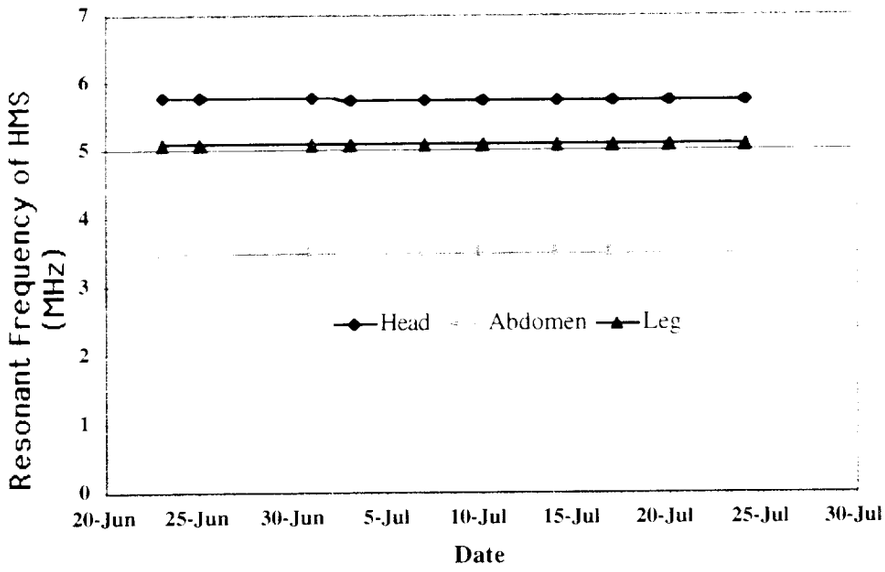


Figure 21: Humidity Measurements over time for Guinea Pig B.

We will continue testing the packages in the guinea pigs weekly and will report further data as it becomes available in the next quarter. The main goal from these tests is to demonstrate that these packages can stay hermetic inside an animal host for a duration upwards of a year. A further implant will be performed on another animal host for a one-month period. This animal will then be sacrificed and a histology examination will be performed in the tissue surrounding the package.

2.6 Automation for In-vitro Testing

To facilitate the in-vitro testing process of anodically-bonded packages incorporated with wireless humidity monitoring systems; an automated testing station is being developed in our laboratory. The system can test up to 96 packages automatically. To measure the resonant frequency of a HMS system inside a package; an external coil, referred to as an antenna, is utilized. The overall system can be divided into two parts: hardware and software.

2.6.1 Hardware

The automation station includes an oven, an impedance analyzer, electromechanical switches, a Personal computer, antennas and packages. The impedance analyzer is used to measure the phase changes of the impedance of an inductively coupled antenna-HMS and to extract its dip phase frequency, which is indeed the resonant frequency of the HMS. Impedance analyzer is connected to the PC through GPIB bus, which controls data transfer between PC and the impedance analyzer DAQcard is a PCI-DIO-96 board, which can control up to 96 switches by its 96 parallel digital output lines, and its I/O connector is connected to switches by cables. The oven is used to keep the packages under a certain preset temperature. Each antenna is connected in series with a switch and all switch-antenna combinations are connected in parallel to the impedance analyzer. The antennas and the silicon-glass packages must be in close proximity to have good coupling and hence a large amplitude for the phase dip. The block diagram of the hardware is shown in Figure 22.

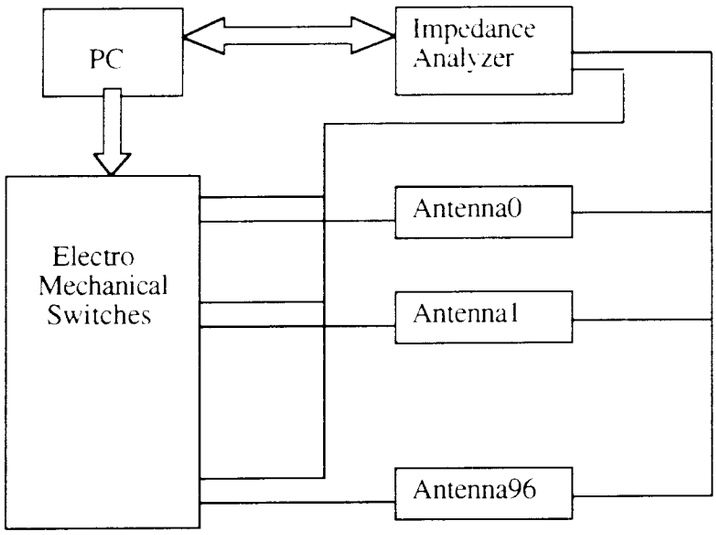


Figure 22: The block diagram of the hardware for the automation station.

2.6.2 Software

To develop the software to operate the system, the commercial LabVIEW program is being used. The PC commands the phase analyzer to initialize analyzing, reads the results saved in the impedance analyzer and stores them in an Excel sheet through LabVIEW. This software uses terminology, icons and ideas familiar to engineers and relies on graphical symbols rather than text language to describe programming action. To explain the software system an overview on how a LabVIEW program works seems necessary.

LabVIEW programs are called Virtual Instruments (VIs), because their appearance and operation imitate actual instruments. A VI has two main parts: front panel and block diagram. Front panel is the interactive user interface of a VI. It contains controls (user inputs) and indicator (program output). Block diagram is the VI's source code. It is the actual executable program. LabVIEW prompts the modular programming concept, so a programmer can divide an application into series of simple subtasks and builds a low-level block diagram to accomplish each subtask and then combine those VIs on a top-level block diagram to complete the larger task. For our application a main VI called automation.vi is created to do the automation task. The main task is divided into subtasks. Different subVIs are created to do these subtasks in sequence. In the first front panel (Figure 23) the user will see a table, whose first 2 columns would show the sweep frequency ranges for the packages and the remaining columns showing the recorded resonant frequencies obtained from previous tests. Accordingly, before each measurement, the user can compare the previously recorded frequencies for each sample. If the operator detects any shift, the second front panel (seen in Figure 24) gives him/her the opportunity to edit the sweep frequency range for any of packages.

The hardware system has been connected and the program has been written. The whole system has been tested and it is fully functional. Currently, we are trying to make the program more user friendly. Also, the present switches seem to have a loading effect on the external antennas, hence we are looking into other types of switches to resolve this problem.

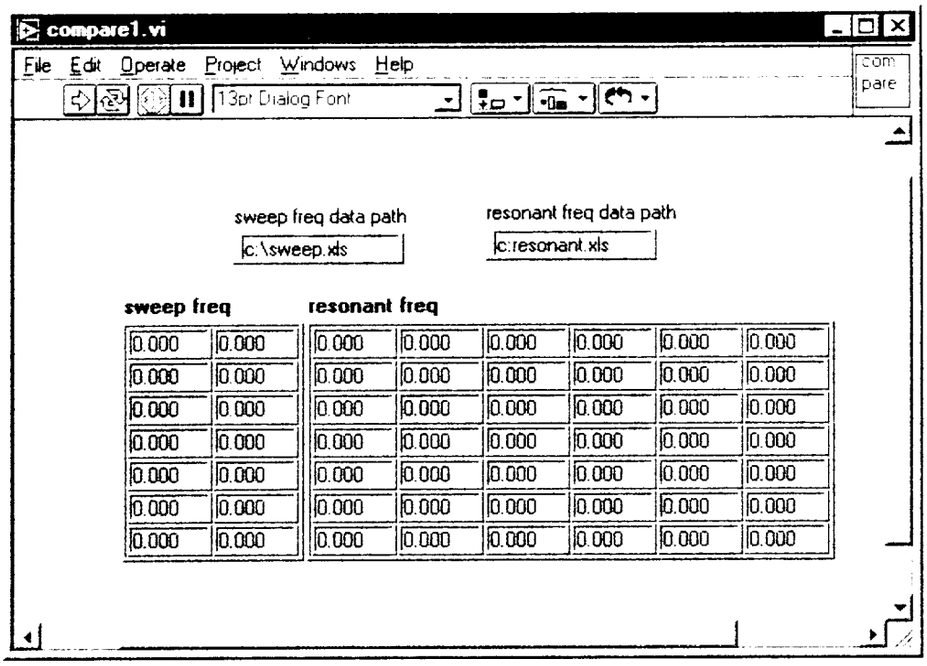


Figure 23: First front panel showing the previously stored values for the resonant frequencies of each package.

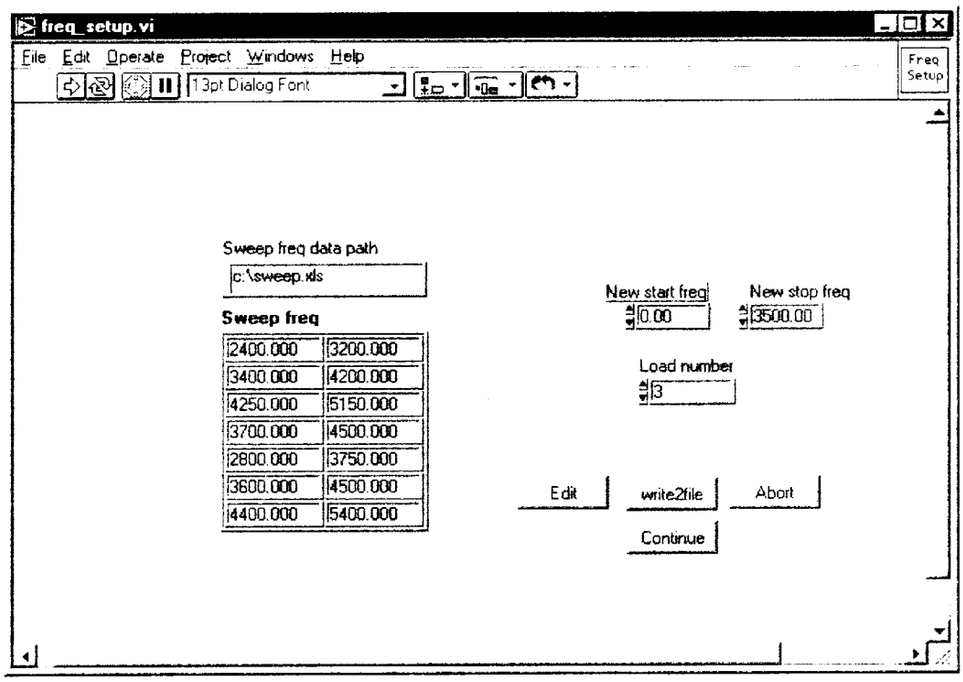


Figure 24: Second front panel that allows the user to adjust the sweep frequency.

2.7 Low Temperature Packaging Techniques for Implantable Microsystems

Packaging of implantable microsystems has so far been realized using silicon-to-glass anodic bonding. The microsystem is, in its most general configuration, composed of a circuit integrated in a silicon chip with the addition of hybrid passive components adhered to the chip and electrical contacts made using wire-bonds. The entire microsystem is subsequently covered with an ultrasonically machined glass capsule and a hermetic bond is achieved at 350 C with about 2000 V applied over the silicon-glass interface [2]. Although this approach satisfies the reliability and hermeticity requirements, it is desirable to seek alternative bonding aproaches that do not require glass and can use silicon as the package cap instead.

The Pyrex #7740 glass used has a temperature coefficient of expansion matched closely to that of silicon up to 400°C. Limiting the bonding temperature to 400°C to avoid stress buildup is not really an impediment, as this is also about the maximum addition to the thermal budget that integrated circuits can withstand. Furthermore, in certain situations where hybrid components (coil or inductors) need to be encapsulated (single channel microstimulator), one also needs to keep the bonding temperatures below 400°C. Proper mating and pre-bonding of the silicon and the glass wafers should force the electric field across the sub-μm interface (which is due to surface irregularities) and not across the much deeper recesses in the glass. Nevertheless ease of handling and manufacturability would favor a silicon-to-silicon bond. An additional advantage of Si-to-Si bonding is the optional microelectronic and/or micromechanical processing of both wafers, which would facilitate the partitioning of system functions over two substrates. A disadvantage could be the absorption in silicon of large parts of the electromagnetic spectrum, which could complicate the implementation of a telemetry link. Within the application area of implantable microsystems, a further analysis of the advantages and disadvantages, along with an inventory of feasible low-temperature and biocompatible Si-to-Si wafer bonding techniques has been detailed below.

2.7.1 Low-temperature intermediate bonding

Conventional Si-to-Si fusion bonding requires exposure of the wafers to about 1000°C. This technique is proven and yields reliable and hermetic bonds [3]. However, the bonding temperature is not compatible with completed microelectronic circuits (circuits failure due to junction outdiffusion or flow of interconnect metal [4]). Similar to glass fusion bonding and anodic bonding in glass a high voltage can be applied across oxidized wafers to enable bonding. However, being able to avoid the critical high-voltage step is one of the motivations that initiated these research efforts. In addition oxygen gas is produced during fusion and anodic bonding [5]. This is a major problem if the bonding technique is to be used to realize an evacuated cavity that contains a high-Q micromechanical resonator, however is not essential in implantable microsystems. Nevertheless, it is considered a drawback. Low-temperature fusion bonding has been demonstrated using fusion bonding at lower temperatures after a special surface activation technique [6]. The results reported do show strong bonds, however no hermeticity.

The limited potential of Si-to-Si fusion bonding in the intended application has resulted in an emphasis on intermediate bonding techniques, in which a third adhesive material is added. The intermediate material can be a polymer (glue), a deposited oxide with a low flowing temperature (that can be used for a subsequent fusion bond), or a metal film.

Polymer-based bonding was not seriously considered. The glue bonding is basically simple; a thin and reasonably uniform layer can be deposited onto the surface using spinning techniques. Pressing the wafers together and subsequent curing results in a bond [7]. However, the glue bond is usually of poor reproducibility due to the limited control of the process. Corrosion due to outgassed products, thermal instability and penetration of moisture limits the reliability. Moreover, the glue adhesion reveals only a limited compatibility with silicon processing.

Glass with a low softening temperature can be deposited on a silicon wafer to serve as an intermediate bonding material. The temperature lowering is basically due to the addition of another substance. The resulting composition shows a phase diagram with an eutectic temperature that is significantly lower than that of pure glass. Bonding using #7570 glass has been reported at 440 C yielding a bonding strength in excess of 1.5 MPa [8]. Spinning sodium silicate as an intermediate layer and an anneal at 200°C for 2 hours results in reliable bonding [9]. The problem in intermediate glass bonding is the thickness control of the intermediate layer. Having a dielectric layer can be an advantage depending on the application. Low-melting point oxides were abandoned because of reliability and reproducibility concerns, and of the existence of non biocompatible materials such as lead.

Metal-based intermediate bonding can be achieved using a wide range of eutectic alloys and solders, however, biocompatibility constraints limit the choice to gold-based eutectics and titanium. Three different techniques are available; eutectic bonding, silicide bonding and solder bonding. In practice these processes are not completely disjunct; e.g. many practical solders are based on a eutectic compound. The silicon-gold compound is usually considered the most promising eutectic combination to realize a eutectic bond, because: (a) of its low eutectic temperature, (b) the widespread use in die-bonding [10] and (c) the compatibility with aluminum interconnect. In this work the proven biocompatibility is considered of even more importance.

2.7.2 Intermediate metal based bonding

Ti [11], TiSi2 [12], PtSi [13] and CoSi2 [14] have been reported to give reliable bonding after an anneal at 700°C. In the case of titanium, a 500 nm layer is E-beam evaporated on both wafers to be bonded. Subsequently, the wafers are brought into contact at room temperature and annealed at 700°C in an oxidizing ambient for 20 minutes [15].

Platinum-silicides can be formed by E-beam evaporation of Pt while keeping the substrate at 350°C. After etching of the Pt layer on top of the formed PtSi, the two wafers to be bonded are brought into contact at room temperature and annealed in a nitrogen ambient for two hours at 700°C. The special property of the silicide-based bond is the good electrical contact between the two bonded wafers.

Eutectic solder based bonding has been reported on an Al-Ge alloy [16]. A 30 atomic % Ge compound enters the eutectic phase at 424°C. The complication in eutectic solder bonding is that the bonding strength also depends on surface adhesion, as the silicon substrate is not involved in the flowing eutectic compound.

Eutectic gold wafer bonding is often promoted due to the minimum in the liquidus line in the Au-Si phase diagram at 363°C for 19 atom.% Si and the widespread use in die bonding [17]. Nevertheless, practical results so far have been poorly reproducible and, therefore, controversial [18-19]. Eutectic gold wafer bonding has also been achieved by local heating [20]. However, the local temperature used was about 800°C. Even though the bonding region requires such a high temperature the rest of the volume inside the package barely see a fraction of this high temperature; however further work needs to be done to characterize the temperature distribution inside the enclosed cavity to discover the usefulness of this technology.

2.7.3 Silicon wafer-to-wafer eutectic bonding

In its most elementary implementation the eutectic Au-Si die bond involves the positioning of a silicon die on a metal layer that is deposited on the package substrate. Applying a contact force and increasing temperature beyond the Au-Si eutectic temperature at 363°C results in diffusion of

silicon into the gold layer, the formation of a eutectic compound at the interface and a eutectic bonding at cool-down. The reliability of such a bond is very limited, due to the oxide that is generally present at the backside of a fully processed silicon wafer. The poor wettability of gold on an oxide surface results in a poor adhesion. Three techniques are available to circumvent this problem:

(a) Rubbing of the silicon die to break the oxide [10]. Obviously a more subtle approach is required in case of a wafer that was subjected to micromachining to realize delicate microstructures.
(b) Removal of the oxide prior to bonding. Unfortunately, a native oxide is already of sufficient thickness to impede adhesion of the gold film. Therefore, a HF clean has to be followed by an argon sputter clean and an in-situ gold sputter deposition to ensure proper gold adhesion [21][22].
(c) Deposition of a thin intermediate metal film that adheres well to the oxide and subsequently a Au layer deposited on top. Suitable intermediate metals are Titanium and Chromium and result in a sub. Si/SiO2/Ti/Au stack or a sub. Si/SiO2/Ti/Au stack.

The second approach is generally adopted in an advanced die bonding process. After backside oxide removal the silicon wafer is backside sputter cleaned and a gold film is in-situ sputter deposited. Subsequently, the metal layer is turned into an Au-Si eutectic alloy by heating up to its eutectic temperature. The package substrate is also Au-coated with a die-attachment preform deposited on top. The preform is usually plated gold, however sometimes a Au-Si eutectic alloy or a softer Pb-Sn eutectic solder is used. Due to the already alloyed interface between the backside of the silicon die and the Au coating, the eutectic die bonding is without any major problem.

The eutectic composition containing 19 atom.% Si is obtained at temperatures beyond 363 °C [17]. Subsequent solidification gives rise to epitaxial growth of both silicon and gold on top of the silicon substrate. The result is composed of numerous small silicon islands protruding a continuous polysilicon gold film [21].

Although the Au adhesion on an atomically clean silicon surface has proven to be a satisfactory solution in die bonding, this technique was not considered in this project, because the equipment was not available. Moreover, the oxide on a circuit wafer to be bonded is for passivation and thus is necessary, which implies that it cannot be removed for wafer bonding convenience. Therefore, the third technique that uses an intermediate adhesive metal is to be applied.

Many metals adhere well to an oxidized silicon surface, however the best known are: aluminum, titanium and chromium. Aluminum is widely used for interconnect, however the Al-Au contact is notorious for forming poorly conductive, brittle silicides at the interface that cause contact failure in case of Au wire bonding to an aluminum interconnect. Therefore, Al is abandoned as an intermediate material. As Ti and Cr are also effective diffusion barriers these are widely applied.

2.7.4 Experimental Results

Structures used for experiments on eutectic gold intermediate bonding were typically composed of a silicon substrate with a 1-200 nm oxide, coated with 20 nm Ti layer and finally a 500-2500 nm Au layer, deposited by evaporation or sputtering. Wafers were bonded after several different cleaning procedures and both in nitrogen flow and on a hot plate in air. Mating of such wafers and subsequent exposure of the wafer pair to a temperature exceeding the Au-Si eutectic temperature have been reported to result in a bond by independent sources [18-19]. The general conclusion that intermediate bonds based on the Au-Ti-Si system are based solely on eutectic alloying at the interface as in the Au-Si system should, however, be reconsidered. The observations are not in agreement with those during bonding at a direct Au-Si interface:

(a) The minimum temperature found for a reliable and uniform bond is significantly higher than the

Au-Si eutectic temperature (520 C versus 363 C). Arguments such as irregular microstructure and temperature gradients over the structure cannot fully account for this difference.
(b) Unlike the case of a Au-Si interface, where silicon and gold are epitaxially grown after solidification, the Au-Ti-Si system results in silicide grains in a gold layer. It seems like in the Si/Ti/Au system the $TiSi_2$ silicide has replaced the silicon.

Simple considerations do support the idea that the incorporation of a Ti intermediate layer should have an effect on the bonding. These materials have been reported to be diffusion barriers and up to some extend that is the reason for their use. However, the very limited solubility of silicon in titanium would prevent the eutectic composition from being reached by diffusion. Moreover, the low-temperature silicidation are bound to complicate the bonding process. These observations indicate that at elevated temperatures silicidation of the Ti layer takes place before reaching the eutectic phase. Silicidation of the Ti is basically similar to the sintering of Al; i.e. the oxide is broken-up by diffusion of silicon into the Ti. In case of Al the silicon is diffused into the Al until saturation occurs or the eutectic phase has been obtained. However, Si does not react with the Al. Ti does react with Si to form a silicide; $TiSi_2$. The local dissolution of the oxide provides direct contact between the gold and the silicon substrate, resulting in the eutectic phase at the interface. The solidification of Au and Si results as the temperature cools down.

As an alternative the use of a Si/Au eutectic solder was investigated. Literature shows that the total layer thickness is critical in achieving a strong bond. In case of the Al/Ge system, a minimum total intermediate layer thickness of 3 μm was reported [16]. Therefore, several values of the layer thickness were used.

Standard silicon wafers were coated with a 200 nm Ti layer using e-beam evaporation. The eutectic compound was deposited on top. The thickness ratio between Si and Au to reach the eutectic composition can be found from:

$$\frac{t_{Si}}{t_{Au}} = \frac{\text{weight\%Si}}{\text{weight\%Au}} \times \frac{\rho_{Au}}{\rho_{Si}} = \frac{3}{97} \times \frac{19.3}{2.32} = 0.25$$

where ρ denotes the density of the material and t is the film thickness. Structures were used with a total intermediate layer thickness between 1 and 5 μm.

The experimental results obtained so far have not been conclusive. The wafers were taken out of the evaporator after deposition of gold and exposed to ambient before the subsequent sputtering of Silicon. Our goal for these tests, have been to try to form a eutectic compound using a deposited layer of Silicon and use this layer as an adhesive layer. Since the Gold target in the sputtering equipment was temporarily inavailable (it was being fixed), and since the evaporator did not have Silicon target, we had to deposit the Ti/Au layers in the evaporator and deposit the final layer using the sputtering equipment. We believe that the waiting period between the time when the wafers were taken out of the evaporator till the time they were loaded into the sputter; the surface of the wafers were contaminated with organic contaminants which made it impossible to give reproducible results using Silicon as an intermediate layer. Furthermore, at temperatures below 450°C, we form a eutectic compound at the top surface with the Silicon coming from substrate in a short period of time. Hence several samples have been undergone this procedure and next been placed on top of each other with some pressure applied from top. As the samples are cooled down, the eutectic metal solidified and we were able to obtain very strong bonds. This was demonstrated using razor blade insertion tests. Again this was mainly an eutectic solder bond between the wafers. We have also tried to achieve a pure eutectic bond by mating a bare silicon wafer with another piece which had a Ti/Au thickness of 500 Å/10,000 Å. The bare Silicon was placed at the bottom and the Silicon with Au metal was placed on top. After a period of several

minutes, one forms a strong eutectic bond observed using a razor blade test. The temperature utilized for these preliminary tests was about 450 C, furthermore more experiments are underway to reduce this temperature. Upon breaking, material should be removed from one wafer to another as seen in Figure 25 below. However, the bond was not uniform around the wafer surface, which is a prerequisite for a hermetic bond. We expect to have more conclusive results after a new run, which will involve in-situ sputtering of gold and silicon.

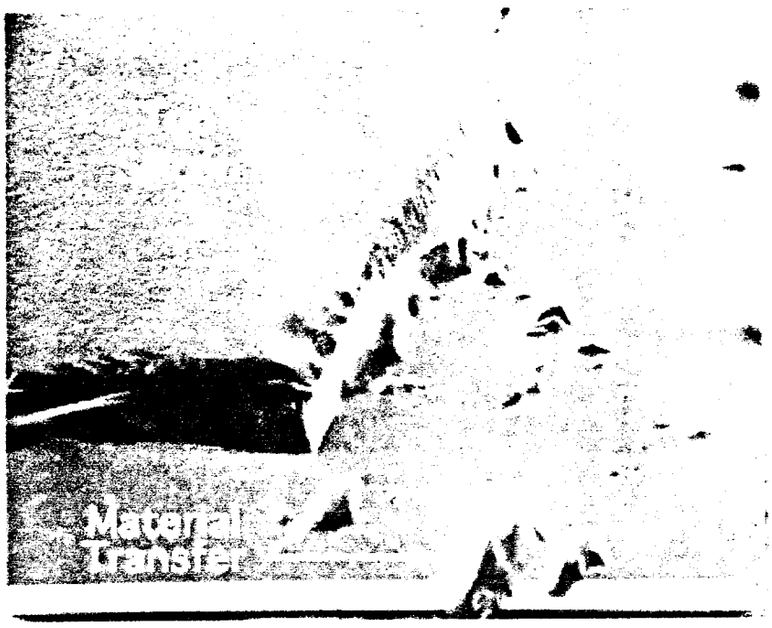


Figure 25: The SEM micrograph of the Silicon samples after being pulled apart.

The actual bonding duration was found to be not of critical value. More reliable bonding was generally achieved when mating the wafers after eutectic flow was visually observed, rather than mating the wafers and assuming eutectic flow after heating of the wafer pair. We have not been able yet to verify the difference between bonding in oxygen ambient or in nitrogen flow, however we expect a significant advantage of bonding in a nitrogen flow, as reported in literature on die bonding [10]. The silicon substrate is not used for supplying the silicon to the compound when using the Si/Au eutectic solder. Therefore, in principle the bonding strength also depends on surface adhesion. The SEM photograph taken after razor insertion indicate that the bond can be stronger than the strength of Si, thus the surface adhesion does not appear to be a problem.

2.7.5 Summary

The options for biocompatible low-temperature silicon-to-silicon wafer bonding for packaging of implantable microsystems have been explored. Intermediate metal-based wafer bonding using eutectic gold was found to have the highest potential in this particular application. Complication in conventional eutectic silicon-gold bonding is that usually a titanium or chromium layer is deposited in between the (oxidized) silicon substrate and the gold layer to ensure adhesion. However, this layer also acts as an effective diffusion barrier. The bonding temperature required is at about 600°C, which is significantly higher than can be expected from the Au-Si phase diagram (eutectic temperature at 363°C). Moreover silicide grains are formed at the bonding interface. It was found that the actual bonding is initiated by the dissolution of the oxide layer by silicidation of the titanium adhesion/barrier layer. The subsequent direct Au-Si contact enables the formation of

the eutectic phase. The silicidation is required to obtain the eutectic alloy with 19 atom.% Si despite the Ti diffusion barrier. This problem is circumvented by the deposition of a Si/Au eutectic solder on top of a Ti layer. The substrate does not play a role and biocompatibility is maintained. Issues addressed are the minimum layer thickness to achieve hermeticity of the bond, the role of oxygen during bonding and the flowing properties of the eutectic melt.

2.7.6 Conclusions

The search for a suitable technique for low-temperature biocompatible Si-to-Si wafer bonding has so far mainly been the elimination of options that do not satisfy the demanding requirements. The analysis shows that the silicon-gold eutectic bond has the highest potential in this application. Initial experiments have demonstrated that the bonding mechanisms involved in the diffusion of silicon from the substrate into the gold to form a eutectic melt are more complex than usually reported. For this reason the emphasis was put on the use of a eutectic Si/Au eutectic solder. First experiments were not conclusive. These demonstrated localized bonding but no hermeticity, due to practical problems with the metal film deposition. Additional experiments are needed to demonstrate the suitability of this technique in encapsulation of implantable microsystems.

2.8 Design and Testing of External Transmitter

In the past quarter, we have made improvements to the class-E transmitter that will be used to power up and send data to the microstimulator and FINESS chips. The schematics of the blocks of the new transmitter design are in Figures 26-28, and a block diagram of the entire transmitter is given in Figure 29. The major addition is the start-up circuitry. In the previous version of the circuit, oscillation did not begin when the power was turned on. This was because initially the output of the comparator was high. This was applied to the gate of M2 and produced the same output from the comparator. To remedy this problem a CMOS oscillator that operates at 4MHz is connected to the gate of M2 via a tri-state buffer.

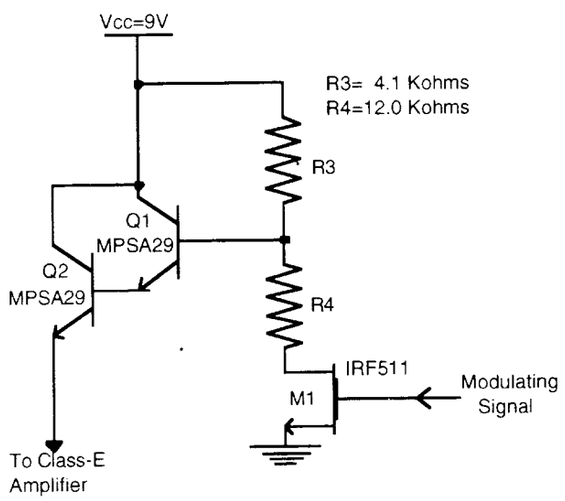
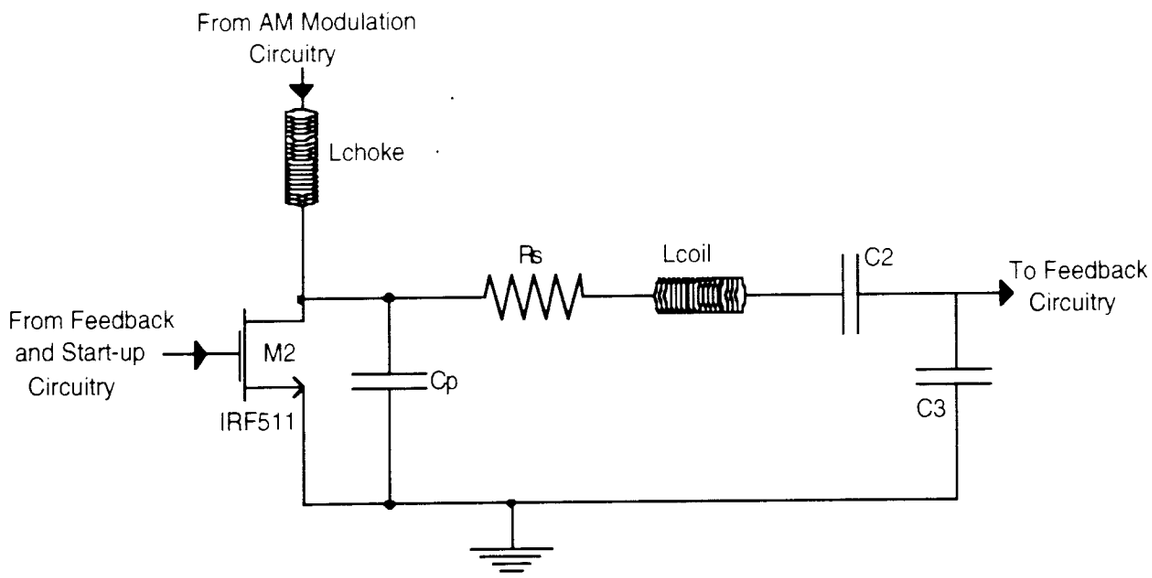


Figure 26: AM circuitry block.



Cp=331 pF
C2= 51 pF
C3= 30 nF
Rs= 4.8 ohms
Lcoil=25.27 uH, Q=392
Lchoke=13.9 uH, Q=73

Figure 27: Class-E amplifier block.

The control signal for this buffer comes from the voltage across capacitor C1. When the power is turned on C1 begins to charge up, and the oscillator is connected to M2 causing the transmitter to oscillate at 4MHz. When the voltage across C1 reaches the switching point of the buffer the CMOS oscillator and the buffer connecting it to the transmitter are turned off, and the class-E amplifier continues to oscillate.

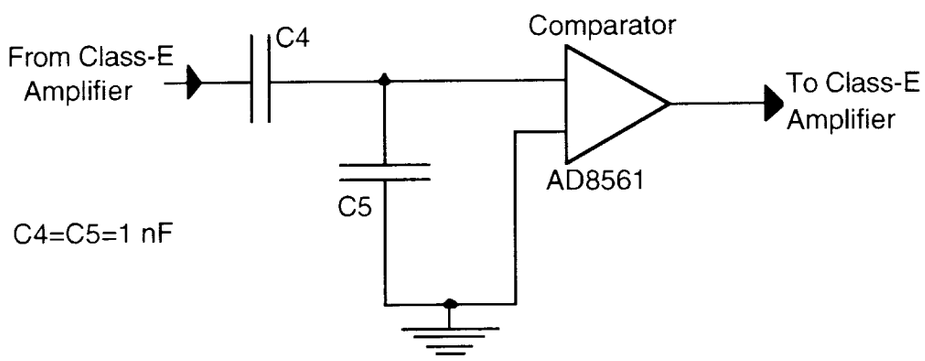


Figure 28: Feedback circuitry block.

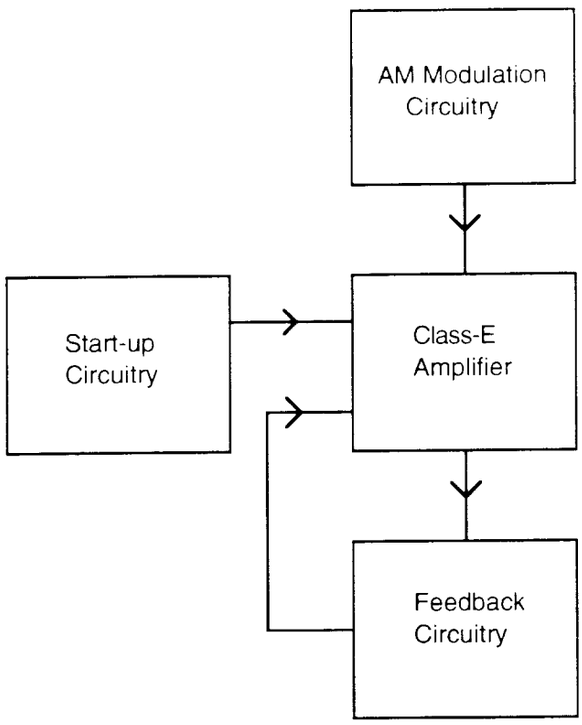


Figure 29: Block diagram of the external transmitter.

Another improvement that has been made in the transmitter is an increase in efficiency. In previous designs of the transmitter at both 2 and 4MHz there was a significantly large amount of power being dissipated in the transistor M2. Because of this, a heat sink was required to keep the transistor cool. In the current design the transistor gets only slightly warm, and is thus dissipating much less power than previous designs. A plot of the gate and drain voltages for the class-E transmitter is given in Figure 30. It can be seen that for the most part the drain voltage is 0V when the gate voltage is high and vice-versa. There is a little bit of time when the transistor is on and there is some drain voltage, and thus there is some power dissipation in the transistor. We would like to have a quantitative measure of efficiency, but to do that one would need to measure the current in the RF choke. Unfortunately even buffered probes present too much of a load to the circuit to be used to measure the choke current. We are currently looking into other ways to quantify the efficiency of the transmitter.

In the FINESS system, the receiving and transmitting coils have a low coupling coefficient because of the large difference in coil size. Because of this, one needs to generate a large voltage in the transmitter coil. The previous class-E transmitter design did not provide a sufficient voltage to the external transmitter coil to power the FINESS chip; it had a maximum value of approximately 60V peak to peak. In the current design this voltage has been increased, and values of greater than 600V can be reached which should be more than necessary. The compromise in achieving this voltage is an increase in the total current drawn from the 9V power supply. The present design draws 260mA of current. This is a problem because the transmitter is intended to be battery operated, and with that much current drawn the battery will not last very long.

While testing the transmitter we noticed that the transmitter coil is significantly loaded when it is close to a person's body. This loading reduces the voltage that can be received by the receiver

coil. This is an important problem to resolve, because in practice the transmitter coils are going to be very close to a person. In the coming quarter, the transmitter will be used to test some of the FINESS chips that have been fabricated, furthermore the coil loading due to close proximity of a person also will be investigated.

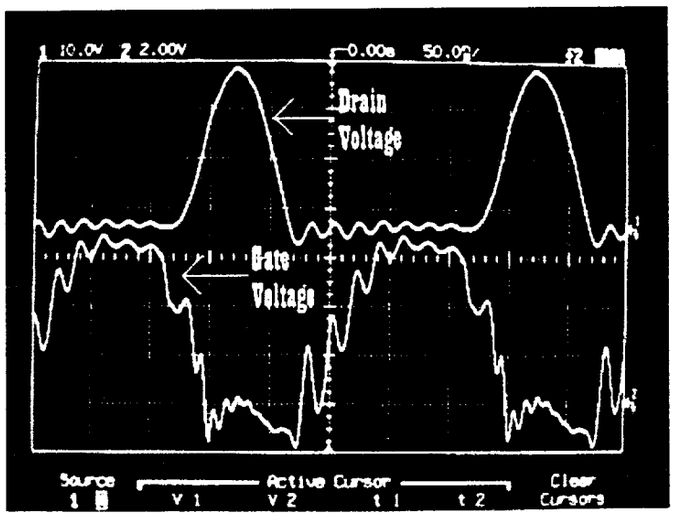


Figure 30: Drain (upper plot) and Gate voltage (lower plot) for the NMOS switch.

III. PLANS FOR THE COMING QUARTER

In the coming quarter, we will finish the fabrication of 2 package substrate wafers employing Boron doping as the dopant for the top polysilicon layer. We will also use electrochemical bias using Au metal for protection against dissolution of polysilicon and then start a set of new soak tests at high temperatures. The automation station will be further optimized and put to use in testing a new set of soak tests at various elevated temperatures. We will implant several glass-silicon packages incorporated with the wireless humidity sensing system into a new guinea pig and continue monitoring the packages that are also presently implanted. We will continue our efforts in looking into alternate low temperature biocompatible bonding/sealing methods for implantable devices as well.

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